LM3445

Triac Dimmable Offline LED Driver

General Description
The LM3445 is an adaptive constant off-time AC/DC buck (step-down) constant current controller designed to be compatible with triac dimmers. The LM3445 provides a constant current for illuminating high power LEDs and includes a triac dim decoder. The dim decoder allows wide range LED dimming using standard triac dimmers. The high frequency capable architecture allows the use of small external passive components. The LM3445 includes a bleeder circuit to ensure proper triac operation by allowing current flow while the line voltage is low to enable proper firing of the triac. A passive PFC circuit ensures good power factor by drawing current directly from the line for most of the cycle, and provides a constant positive voltage to the buck regulator. Additional features include thermal shutdown, current limit and $V_{CC}$ under-voltage lockout.

Features
- Triac dim decoder circuit for LED dimming
- Application voltage range $80V_{AC} \rightarrow 277V_{AC}$
- Capable of controlling LED currents greater than 1A
- Adjustable switching frequency
- Low quiescent current
- Adaptive programmable off-time allows for constant ripple current
- Thermal shutdown
- No 120Hz flicker
- Low profile 10 pin MSOP Package or 14 pin SOIC
- Patent pending drive architecture

Applications
- Retro Fit Triac Dimming
- Solid State Lighting
- Industrial and Commercial Lighting
- Residential Lighting

Typical LM3445 LED Driver Application Circuit

![Typical LM3445 LED Driver Application Circuit](image)
Connection Diagrams

Ordering Information

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Spec.</th>
<th>Package Type</th>
<th>NSC Package Drawing</th>
<th>Top Mark</th>
<th>Supplied As</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3445MM</td>
<td>NOPB</td>
<td>MSOP-10</td>
<td>MUB10A</td>
<td>SULB</td>
<td>1000 Units, Tape and Reel</td>
</tr>
<tr>
<td>LM3445MX</td>
<td>NOPB</td>
<td>MSOP-10</td>
<td>MUB10A</td>
<td>SULB</td>
<td>3500 Units, Tape and Reel</td>
</tr>
<tr>
<td>LM3445M</td>
<td>NOPB</td>
<td>SOIC-14L</td>
<td>M14A</td>
<td>LM3445M</td>
<td>55 Units, Rail</td>
</tr>
<tr>
<td>LM3445MX</td>
<td>NOPB</td>
<td>SOIC-14L</td>
<td>M14A</td>
<td>LM3445M</td>
<td>2500 Units, Tape and Reel</td>
</tr>
</tbody>
</table>

Pin Descriptions

<table>
<thead>
<tr>
<th>SOIC</th>
<th>MSOP</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>1</td>
<td>ASNS</td>
<td>PWM output of the triac dim decoder circuit. Outputs a 0 to 4V PWM signal with a duty cycle proportional to the triac dimmer on-time.</td>
</tr>
<tr>
<td>13</td>
<td>2</td>
<td>FLTR1</td>
<td>First filter input. The 120Hz PWM signal from ASNS is filtered to a DC signal and compared to a 1 to 3V, 5.85 kHz ramp to generate a higher frequency PWM signal with a duty cycle proportional to the triac dimmer firing angle. Pull above 4.9V (typical) to tri-state DIM.</td>
</tr>
<tr>
<td>14</td>
<td>3</td>
<td>DIM</td>
<td>Input/output dual function dim pin. This pin can be driven with an external PWM signal to dim the LEDs. It may also be used as an output signal and connected to the DIM pin of other LM3445s or other LED drivers to dim multiple LED circuits simultaneously.</td>
</tr>
<tr>
<td>1</td>
<td>4</td>
<td>COFF</td>
<td>OFF time setting pin. A user set current and capacitor connected from the output to this pin sets the constant OFF time of the switching controller.</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>FLTR2</td>
<td>Second filter input. A capacitor tied to this pin filters the PWM dimming signal to supply a DC voltage to control the LED current. Could also be used as an analog dimming input.</td>
</tr>
<tr>
<td>4</td>
<td>6</td>
<td>GND</td>
<td>Circuit ground connection.</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>ISNS</td>
<td>LED current sense pin. Connect a resistor from main switching MOSFET source, ISNS to GND to set the maximum LED current.</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>GATE</td>
<td>Power MOSFET driver pin. This output provides the gate drive for the power switching MOSFET of the buck controller.</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
<td>VCC</td>
<td>Input voltage pin. This pin provides the power for the internal control circuitry and gate driver.</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>BLDR</td>
<td>Bleeder pin. Provides the input signal to the angle detect circuitry as well as a current path through a switched 230Ω resistor to ensure proper firing of the triac dimmer.</td>
</tr>
<tr>
<td>2,5,6,11</td>
<td>-</td>
<td>N/C</td>
<td>No Connect</td>
</tr>
</tbody>
</table>

www.ti.com
Absolute Maximum Ratings (Note 1)  
If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Condition</th>
<th>BLDR to GND</th>
<th>VCC, GATE, FLTR1 to GND</th>
<th>ISNS to GND</th>
<th>GND, ASNS, DIM, FLTR2, COFF</th>
<th>Continuously Power Dissipation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Range</td>
<td>0.3V to +17V</td>
<td>0.3V to +14V</td>
<td>0.3V to +2.5V</td>
<td>-0.3V to +7.0V</td>
<td>Internally Limited</td>
</tr>
</tbody>
</table>

ESD Susceptibility (Note 3)  
<table>
<thead>
<tr>
<th>Type</th>
<th>HBM</th>
<th>Junction Temperature (TJ-MAX)</th>
<th>Storage Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level</td>
<td>2 kV</td>
<td>150°C</td>
<td>-65°C to +150°C</td>
</tr>
</tbody>
</table>

Operating Conditions  
<table>
<thead>
<tr>
<th>Condition</th>
<th>VCC</th>
<th>Junction Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Range</td>
<td>8.0V to 12V</td>
<td>−40°C to +125°C</td>
</tr>
</tbody>
</table>

Electrical Characteristics  
Limits in standard type face are for Tj = 25°C and those with boldface type apply over the full Operating Temperature Range (Tj = −40°C to +125°C). Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at Tj = +25°C, and are provided for reference purposes only.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLEEDER</td>
<td>RBLDR</td>
<td>Bleeder resistance to GND</td>
<td>BLDR = 10mA</td>
<td>230</td>
<td>325</td>
<td>Ω</td>
</tr>
<tr>
<td>VCC SUPPLY</td>
<td>I VCC</td>
<td>Operating supply current</td>
<td></td>
<td>2.00</td>
<td>2.85</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>VCC-UVLO</td>
<td>Rising threshold</td>
<td></td>
<td>7.4</td>
<td>7.7</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling threshold</td>
<td></td>
<td>6.0</td>
<td>6.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hysterisis</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>COFF</td>
<td>VCOFF</td>
<td>Time out threshold</td>
<td></td>
<td>1.225</td>
<td>1.276</td>
<td>1.327</td>
</tr>
<tr>
<td></td>
<td>RCOFF</td>
<td>Off timer sinking impedance</td>
<td></td>
<td>33</td>
<td>60</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>ICOFF</td>
<td>Restart timer</td>
<td></td>
<td>180</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>CURRENT LIMIT</td>
<td>VISNS</td>
<td>ISNS limit threshold</td>
<td></td>
<td>1.174</td>
<td>1.269</td>
<td>1.364</td>
</tr>
<tr>
<td></td>
<td>ISNS</td>
<td>Leading edge blanking time</td>
<td></td>
<td>125</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Current limit reset delay</td>
<td></td>
<td>180</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ISNS limit to GATE delay</td>
<td>ISNS = 0 to 1.75V step</td>
<td>33</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>INTERNAL PWM RAMP</td>
<td>FRAMP</td>
<td>Frequency</td>
<td></td>
<td>5.85</td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>VRAMP</td>
<td>Valley voltage</td>
<td></td>
<td>0.96</td>
<td>1.00</td>
<td>1.04</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Peak voltage</td>
<td></td>
<td>2.85</td>
<td>3.00</td>
<td>3.08</td>
</tr>
<tr>
<td></td>
<td>DRAMP</td>
<td>Maximum duty cycle</td>
<td></td>
<td>96.5</td>
<td>98.0</td>
<td></td>
</tr>
<tr>
<td>DIM DECODER</td>
<td>FANL_DET</td>
<td>Angle detect rising threshold</td>
<td>Observed on BLDR pin</td>
<td></td>
<td>6.79</td>
<td>7.21</td>
</tr>
<tr>
<td></td>
<td>VASNS</td>
<td>ASNS filter delay</td>
<td></td>
<td>4</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ASNS VMAX</td>
<td></td>
<td>3.85</td>
<td>4.00</td>
<td>4.15</td>
</tr>
<tr>
<td></td>
<td>IASNS</td>
<td>ASNS drive capability sink</td>
<td>VASNS = 2V</td>
<td>7.6</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ASNS drive capability source</td>
<td>VASNS = 2V</td>
<td>-4.3</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DIM low sink current</td>
<td>VDIM = 1V</td>
<td>1.65</td>
<td>2.80</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DIM High source current</td>
<td>VDIM = 4V</td>
<td>-4.00</td>
<td>-3.00</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VDIM</td>
<td>DIM low voltage</td>
<td>PWM input voltage threshold</td>
<td></td>
<td>0.9</td>
<td>1.33</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DIM high voltage</td>
<td></td>
<td>2.33</td>
<td>3.15</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VTSTH</td>
<td>Tri-state threshold voltage</td>
<td>Apply to FLTR1 pin</td>
<td></td>
<td>4.87</td>
<td>5.25</td>
</tr>
<tr>
<td></td>
<td>RDIM</td>
<td>DIM comparator tri-state impedance</td>
<td></td>
<td>10</td>
<td></td>
<td>MΩ</td>
</tr>
<tr>
<td>Symbol</td>
<td>Parameter</td>
<td>Conditions</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Units</td>
</tr>
<tr>
<td>----------</td>
<td>------------------------------------</td>
<td>---------------------</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
</tr>
<tr>
<td></td>
<td><strong>CURRENT SENSE COMPARATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{FLTR2}} )</td>
<td>FLTR2 open circuit voltage</td>
<td></td>
<td>720</td>
<td>750</td>
<td>780</td>
<td>mV</td>
</tr>
<tr>
<td>( R_{\text{FLTR2}} )</td>
<td>FLTR2 impedance</td>
<td></td>
<td>420</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>( V_{\text{OS}} )</td>
<td>Current sense comparator offset voltage</td>
<td></td>
<td>-4.0</td>
<td>0.1</td>
<td>4.0</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td><strong>GATE DRIVE OUTPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{DRVH}} )</td>
<td>GATE high saturation ( I_{\text{GATE}} = 50 \text{ mA} )</td>
<td></td>
<td>0.24</td>
<td>0.50</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{DRVL}} )</td>
<td>GATE low saturation ( I_{\text{GATE}} = 100 \text{ mA} )</td>
<td></td>
<td>0.22</td>
<td>0.50</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{\text{DRV}} )</td>
<td>Peak source current ( \text{GATE} = \frac{V_{\text{CC}}}{2} )</td>
<td></td>
<td>-0.77</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Peak sink current ( \text{GATE} = \frac{V_{\text{CC}}}{2} )</td>
<td></td>
<td>0.88</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{\text{DV}} )</td>
<td>Rise time</td>
<td>( C_{\text{load}} = 1 \text{ nF} )</td>
<td>15</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Fall time</td>
<td>( C_{\text{load}} = 1 \text{ nF} )</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>THERMAL SHUTDOWN</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_{\text{SD}} )</td>
<td>Thermal shutdown temperature ( \text{(Note 4)} )</td>
<td></td>
<td>165</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Thermal shutdown hysteresis</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{\text{JA}} )</td>
<td>MSOP-10 junction to ambient</td>
<td></td>
<td>121</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
</tbody>
</table>

**Note 1:** Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics. All voltages are with respect to the potential at the GND pin, unless otherwise specified.

**Note 2:** Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at \( T_{J} = 165°C \) (typ.) and disengages at \( T_{J} = 145°C \) (typ.).

**Note 3:** Human Body Model, applicable std. JESD22-A114-C.

**Note 4:** Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature \( (T_{A-MAX}) \) is dependent on the maximum operating junction temperature \( (T_{J-MAX-OP} = 125°C) \), the maximum power dissipation of the device in the application \( (P_{D-MAX}) \), and the junction-to ambient thermal resistance of the part/package in the application \( (R_{JA}) \), as given by the following equation: \( T_{A-MAX} = T_{J-MAX-OP} - (R_{JA} \times P_{D-MAX}) \).
Typical Performance Characteristics

- **f_{SW} vs Input Line Voltage**
  - 7 LEDs in Series \( V_O = 24.5 \text{V} \)
  - \( C_{11} = 2.2 \text{nF}, R_3 = 348 \text{k}\Omega \)

- **Efficiency vs Input Line Voltage**
  - 14 Series connected LEDs
  - 10 Series connected LEDs

- **BLDR Resistor vs Temperature**

- **V_{CC} UVLO vs Temperature**
  - UVLO (V_{CC}) Rising
  - UVLO (V_{CC}) Falling

- **Min On-Time (t_{ON}) vs Temperature**

- **Off Threshold (C11) vs Temperature**
  - OFF Threshold at C11
Normalized Variation in $f_{SW}$ over $V_{BUCK}$ Voltage

Leading Edge Blanking Variation Over Temperature
FIGURE 1. Simplified Block Diagram
Application Information

FUNCTIONAL DESCRIPTION
The LM3445 contains all the necessary circuitry to build a line-powered (mains powered) constant current LED driver whose output current can be controlled with a conventional triac dimmer.

OVERVIEW OF PHASE CONTROL DIMMING
A basic "phase controlled" triac dimmer circuit is shown in Figure 2.

![Figure 2. Basic Triac Dimmer](image)

An RC network consisting of R1, R2, and C1 delay the turn on of the triac until the voltage on C1 reaches the trigger voltage of the diac. Increasing the resistance of the potentiometer (wiper moving downward) increases the turn-on delay which decreases the on-time or "conduction angle" of the triac (θ). This reduces the average power delivered to the load. Voltage waveforms for a simple triac dimmer are shown in Figure 3. Figure 3a shows the full sinusoid of the input voltage. Even when set to full brightness, few dimmers will provide 100% on-time, i.e., the full sinusoid.

![Figure 3. Line Voltage and Dimming Waveforms](image)

Figure 3b shows a theoretical waveform from a dimmer. The on-time is often referred to as the "conduction angle" and may be stated in degrees or radians. The off-time represents the delay caused by the RC circuit feeding the triac. The off-time be referred to as the "firing angle" and is simply 180° - θ.

Figure 3c shows a waveform from a so-called reverse phase dimmer, sometimes referred to as an electronic dimmer. These typically are more expensive, microcontroller based dimmers that use switching elements other than triacs. Note that the conduction starts from the zero-crossing, and terminates some time later. This method of control reduces the noise spike at the transition.

Since the LM3445 has been designed to assess the relative on-time and control the LED current accordingly, most phase-control dimmers, both forward and reverse phase, may be used with success.
Theory of Operation
Refer to figure 4 below which shows the LM3445 along with basic external circuitry.

FIGURE 4. LM3445 Schematic
SENSING THE RECTIFIED TRIAC WAVEFORM
A bridge rectifier, BR1, converts the line (mains) voltage (5c) into a series of half-sines as shown in 5b. Figure 5a shows a typical voltage waveform after diode D3 (valley fill circuit, or $V_{BUCK}$).

**FIGURE 5. Voltage Waveforms After Bridge Rectifier Without Triac Dimming**

Figure 6c and 6b show typical triac dimmed voltage waveforms before and after the bridge rectifier. Figure 6a shows a typical triac dimmed voltage waveform after diode D3 (valley fill circuit, or $V_{BUCK}$).

**FIGURE 6. Voltage Waveforms After Bridge Rectifier With Triac Dimming**

LM3445 LINE SENSING CIRCUITRY
An external series pass regulator (R2, D1, and Q1) translates the rectified line voltage to a level where it can be sensed by the BLDR pin on the LM3445.

**FIGURE 7. LM3445 AC Line Sense Circuitry**

D1 is typically a 15V zener diode which forces transistor Q1 to "stand-off" most of the rectified line voltage. Having no capacitance on the source of Q1 allows the voltage on the BLDR pin to rise and fall with the rectified line voltage as the line voltage drops below zener voltage D1 (see the section on Angle Detect).

A diode-capacitor network (D2, C5) is used to maintain the voltage on the VCC pin while the voltage on the BLDR pin goes low. This provides the supply voltage to operate the LM3445.

Resistor R5 is used to bleed charge out of any stray capacitance on the BLDR node and may be used to provide the necessary holding current for the dimmer when operating at light output currents.

TRIAC HOLDING CURRENT RESISTOR
In order to emulate an incandescent light bulb (essentially a resistor) with any LED driver, the existing triac will require a small amount of holding current throughout the AC line cycle. An external resistor (R5) needs to be placed on the source of Q1 to GND to perform this function. Most existing triac dimmers only require a few milliamps of current to hold them on.

A few "less expensive" triacs sold on the market will require a bit more current. The value of resistor R5 will depend on:

- What type of triac the LM3445 will be used with
- How many light fixtures are running off of the triac

With a single LM3445 circuit on a common triac dimmer, a holding current resistor between 3 kΩ and 5 kΩ will be required. As the number of LM3445 circuits is added to a single dimmer, the holding resistor R5’s resistance can be increased. A few triac dimmers will require a resistor as low as 1 kΩ or lower for a single LM3445 circuit. The trade-off will be
performance vs efficiency. As the holding resistor R5 is increased, the overall efficiency per LM3445 will also increase.

ANGLE DETECT
The Angle Detect circuit uses a comparator with a fixed threshold voltage of 7.21V to monitor the BLDR pin to determine whether the triac is on or off. The output of the comparator drives the ASNS buffer and also controls the Bleeder circuit. A 4 μs delay line on the output is used to filter out noise that could be present on this signal.

The output of the Angle Detect circuit is limited to a 0V to 4.0V swing by the buffer and presented to the ASNS pin. R1 and C3 comprise a low-pass filter with a bandwidth on the order of 1.0Hz.

The Angle Detect circuit and its filter produce a DC level which corresponds to the duty cycle (relative on-time) of the triac dimmer. As a result, the LM3445 will work equally well with 50Hz or 60Hz line voltages.

BLEEDER
While the BLDR pin is below the 7.21V threshold, the bleeder MOSFET is biased to place a small load (230 Ω) on the series pass regulator. This additional load is necessary to complete the circuit through the triac dimmer so that the dimmer delay circuit can operate correctly. Above 7.21V, the bleeder resistor is removed to increase efficiency.

FLTR1 PIN
The FLTR1 pin has two functions. Normally, it is fed by ASNS through filter components R1 and C3 and drives the dim decoder. However, if the FLTR1 pin is tied above 4.9V (typical), e.g., to VCC, the Ramp Comparator is tri-stated, disabling the dim decoder. See the Master/Slave section.

DIM DECODER
The ramp generator produces a 5.85 kHz saw tooth wave with a minimum of 1.0V and a maximum of 3.0V. The filtered ASNS signal enters pin FLTR1 where it is compared against the output of the Ramp Generator.

The output of the ramp comparator will have an on-time which is inversely proportional to the average voltage level at pin FLTR1. However, since the FLTR1 signal can vary between 0V and 4.0V (the limits of the ASNS pin), and the Ramp Generator signal only varies between 1.0V and 3.0V, the output of the ramp comparator will be on continuously for V_{FLTR1} < 1.0V and off continuously for V_{FLTR1} > 3.0V. This allows a decoding range from 45° to 135° to provide a 0 – 100% dimming range.

The output of the ramp comparator drives both a common-source N-channel MOSFET through a Schmitt trigger and the DIM pin (see the Master/Slave section for further functions of the DIM pin). The MOSFET drain is pulsed up to 750 mV by a 50 kΩ resistor.

Since the MOSFET inverts the output of the ramp comparator, the drain voltage of the MOSFET is proportional to the duty cycle of the line voltage that comes through the triac dimmer. The amplitude of the ramp generator causes this proportionality to "hard limit" for duty cycles above 75% and below 25%.

The MOSFET drain signal next passes through an RC filter comprised of an internal 370 kΩ resistor, and an external capacitor on pin FLTR2. This forms a second low pass filter to further reduce the ripple in this signal, which is used as a reference by the PWM comparator. This RC filter is generally set to 10Hz.

The net effect is that the output of the dim decoder is a DC voltage whose amplitude varies from near 0V to 750 mV as the duty cycle of the dimmer varies from 25% to 75%. This corresponds to conduction angles of 45° to 135°, respectively.

The output voltage of the Dim Decoder directly controls the peak current that will be delivered by Q2 during its on-time. See the Buck Converter section for details.

As the triac fires beyond 135°, the DIM decoder no longer controls the dimming. At this point the LEDs will dim gradually for one of two reasons:

1. The voltage at V_{Buck} decreases and the buck converter runs out of headroom and causes LED current to decrease as V_{Buck} decreases.
2. Minimum on-time is reached which fixes the duty-cycle and therefore reduces the voltage at V_{Buck}.

The transition from dimming with the DIM decoder to headroom or minimum on-time dimming is seamless. LED currents from full load to as low as 0.5 mA can be easily achieved.

VALLEY-FILL CIRCUIT
V_{Buck} supplies the power which drives the LED string. Diode D3 allows V_{Buck} to remain high while V+ cycles on and off. V_{Buck} has a relatively small hold capacitor C10 which reduces the voltage ripple when the valley fill capacitors are being charged. However, the network of diodes and capacitors shown between D3 and C10 make up a "valley-fill" circuit. The valley-fill circuit can be configured with two or three stages. The most common configuration is two stages. Figure 8 illustrates a two and three stage valley-fill circuit.

![FIGURE 8. Two and Three Stage Valley Fill Circuit](30060318)
The valley-fill circuit allows the buck regulator to draw power throughout a larger portion of the AC line. This allows the capacitance needed at \( V_{\text{BUCK}} \) to be lower than if there were no valley-fill circuit, and adds passive power factor correction (PFC) to the application. Besides better power factor correction, a valley-fill circuit allows the buck converter to operate while separate circuitry translates the dimming information. This allows for dimming that isn’t subject to 120Hz flicker that can be perceived by the human eye.

**VALLEY-FILL OPERATION**

When the “input line is high”, power is derived directly through D3. The term “input line is high” can be explained as follows. The valley-fill circuit charges capacitors C7 and C9 in series (see figure 9) when the input line is high.

![Figure 9. Two stage Valley-Fill Circuit when AC Line is High](image)

The peak voltage of a two stage valley-fill capacitor is:

\[
V_{\text{VF-CAP}} = \frac{V_{\text{AC-RMS}}\sqrt{2}}{2}
\]

As the AC line decreases from its peak value every cycle, there will be a point where the voltage magnitude of the AC line is equal to the voltage that each capacitor is charged. At this point diode D3 becomes reversed biased, and the capacitors are placed in parallel to each other (figure 10), and \( V_{\text{BUCK}} \) equals the capacitor voltage.

![Figure 10. Two stage Valley-Fill Circuit when AC Line is Low](image)

A three stage valley-fill circuit performs exactly the same as two-stage valley-fill circuit except now three capacitors are now charged in series, and when the line voltage decreases to:

\[
V_{\text{VF-CAP}} = \frac{V_{\text{AC-RMS}}\sqrt{2}}{3}
\]

Diode D3 is reversed biased and three capacitors are in parallel to each other.

The valley-fill circuit can be optimized for power factor, voltage hold up and overall application size and cost. The LM3445 will operate with a single stage or a three stage valley-fill circuit as well. Resistor R8 functions as a current limiting resistor during start-up, and during the transition from series to parallel connection. Resistors R6 and R7 are 1 MΩ bleeder resistors, and may or may not be necessary for each application.

**BUCK CONVERTER**

The LM3445 is a buck controller that uses a proprietary constant off-time method to maintain constant current through a string of LEDs. While transistor Q2 is on, current ramps up through the inductor and LED string. A resistor R3 senses this current and this voltage is compared to the reference voltage at FLTR2. When this sensed voltage is equal to the reference voltage, transistor Q2 is turned off and diode D10 conducts the current through the inductor and LEDs. Capacitor C12 eliminates most of the ripple current seen in the inductor. Resistor R4, capacitor C11, and transistor Q3 provide a linear current ramp that sets the constant off-time for a given output voltage.
OVERVIEW OF CONSTANT OFF-TIME CONTROL

A buck converter’s conversion ratio is defined as:

\[ \frac{V_O}{V_{IN}} = D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times f_{SW} \]

Constant off-time control architecture operates by simply defining the off-time and allowing the on-time, and therefore the switching frequency, to vary as either \(V_{IN}\) or \(V_O\) changes. The output voltage is equal to the LED string voltage (\(V_{LED}\)), and should not change significantly for a given application. The input voltage or \(V_{BUCK}\) in this analysis will vary as the input line varies. The length of the on-time is determined by the sensed inductor current through a resistor to a voltage reference at a comparator. During the on-time, denoted by \(t_{ON}\), MOSFET switch Q2 is on causing the inductor current to increase. During the on-time, current flows from \(V_{BUCK}\) through the LEDs, through L2, Q2, and finally through R3 to ground. At some point in time, the inductor current reaches a maximum (\(I_{L2-PK}\)) determined by the voltage sensed at R3 and the ISNS pin. This sensed voltage across R3 is compared against the voltage of dim decoder output, FLTR2, at which point Q2 is turned off by the controller.

During the off-period denoted by \(t_{OFF}\), the current through L2 continues to flow through the LEDs via D10.
MASTER/SLAVE OPERATION
Multiple LM3445s can be configured so that large strings of LEDs can be controlled by a single triac dimmer. By doing so, smooth consistent dimming for multiple LED circuits is achieved.

When the FLTR1 pin is tied above 4.9V (typical), preferably to VCC, the ramp comparator is tri-stated, disabling the dim decoder. This allows one or more LM3445 devices or PWM LED driver devices (slaves) to be controlled by a single LM3445 (master) by connecting their DIM pins together.

MASTER/SLAVE CONFIGURATION
National Semiconductor offers an LM3445 demonstration PCB for customer evaluation through our website. The following description and theory uses reference designators that follow our evaluation PCB. The LM3445 Master/Slave schematics are illustrated below (figures 13 - 15) for clarity. Each board contains a separate circuit for the Master and Slave function. Both the Master and Slave boards will need to be modified from their original stand alone function so that they can be coupled together. Only the Master LM3445 requires use of the Master/Slave circuit for any number of slaves.

MASTER BOARD MODIFICATIONS
- Remove R10 and replace with a BAS40 diode
- Connect TP18 to TP14 (VCC)
- Connect TP17 (gate of Q5) to TP15 (gate of Q2)

SLAVE BOARD(S) MODIFICATIONS
- Remove R11 (disconnects BLDR)
- Tie TP14 (FLTR1) to VCC

MASTER/SLAVE(S) INTERCONNECTION
- Connect TP19 of Master to TP10 of Slave (Master VCC Control)
- Connect TP6 (DIM pin) of Master to TP6 (DIM pin) of Slave (Master DIM Control)

MASTER/SLAVE THEORY OF OPERATION
By placing two series diodes on the Master VCC circuit one forces the master VCC UVLO to become the dominant threshold. When Master VCC drops below UVLO, GATE stops switching and the RC timer (>200 µs) rises above the TL431 threshold (2.5V) which in turn pulls down on the gate of the Slave pass device (Q1).

The valley-fill circuit could consist of one large circuit to power all LM3445 series connected, or each LM3445 circuit could have a separate valley-fill circuit located near the buck converter.
**FIGURE 13. Master Slave Configuration**

**FIGURE 14. Master/Slave configuration with Separate Valley-Fill Circuits**
FIGURE 15. Master/Slave configuration with One Valley-Fill Circuit

THERMAL SHUTDOWN
Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch doesn’t turn on until the junction temperature drops to approximately 145°C.
Design Guide

DETERMINING DUTY-CYCLE (D)
Duty cycle (D) approximately equals:

\[
\frac{V_{LED}}{V_{BUCK}} = D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times f_{SW}
\]

With efficiency considered:

\[
\frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}} = D
\]

For simplicity, choose efficiency between 75% and 85%.

CALCULATING OFF-TIME
The “Off-Time” of the LM3445 is set by the user and remains fairly constant as long as the voltage of the LED stack remains constant. Calculating the off-time is the first step in determining the switching frequency of the converter, which is integral in determining some external component values.

PNP transistor Q3, resistor R4, and the LED string voltage define a charging current into capacitor C11. A constant current into a capacitor creates a linear charging characteristic.

\[
i = C \frac{dv}{dt}
\]

Resistor R4, capacitor C11 and the current through resistor R4 (\(i_{COLL}\)), which is approximately equal to \(V_{LED}/R4\), are all fixed. Therefore, \(dv\) is fixed and linear, and \(dt\) (\(t_{OFF}\)) can now be calculated.

\[
t_{OFF} = C11 \times 1.276V \times \left( \frac{R4}{V_{LED}} \right)
\]

Common equations for determining duty cycle and switching frequency in any buck converter:

\[
f_{SW} = \frac{1}{t_{OFF} + t_{ON}}
\]

\[
D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_{LED}}{V_{BUCK}}
\]

\[
D' = \frac{t_{OFF}}{t_{ON} + t_{OFF}}
\]

Therefore:

\[
f_{SW} = \frac{D}{t_{ON}}, \text{ and } f_{SW} = \frac{1 - D}{t_{OFF}}
\]

With efficiency of the buck converter in mind:

\[
\frac{V_{LED}}{V_{BUCK}} = \eta \times D
\]

Substitute equations and rearrange:

\[
f_{SW} = \frac{1}{t_{OFF}} \left( 1 - \frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}} \right)
\]

Off-time, and switching frequency can now be calculated using the equations above.

SETTING THE SWITCHING FREQUENCY
Selecting the switching frequency for nominal operating conditions is based on tradeoffs between efficiency (better at low frequency) and solution size/cost (smaller at high frequency). The input voltage to the buck converter (\(V_{BUCK}\)) changes with both line variations and over the course of each half-cycle of the input line voltage. The voltage across the LED string will, however, remain constant, and therefore the off-time remains constant.

The on-time, and therefore the switching frequency, will vary as the \(V_{BUCK}\) voltage changes with line voltage. A good design practice is to choose a desired nominal switching frequency knowing that the switching frequency will decrease as the line voltage drops and increase as the line voltage increases (see figure 16).

FIGURE 16. Graphical Illustration of Switching Frequency vs \(V_{BUCK}\)
The off-time of the LM3445 can be programmed for switching frequencies ranging from 30 kHz to over 1 MHz. A trade-off between efficiency and solution size must be considered when designing the LM3445 application.

The maximum switching frequency attainable is limited only by the minimum on-time requirement (200 ns).

Worst case scenario for minimum on time is when $V_{\text{BUCK}}$ is at its maximum voltage (AC high line) and the LED string voltage ($V_{\text{LED}}$) is at its minimum value.

$$t_{\text{ON(MIN)}} = \left( \frac{1}{\eta} \times \frac{V_{\text{LED(MIN)}}}{V_{\text{BUCK(MAX)}}} \right) \times \frac{1}{f_{\text{SW}}}$$

The maximum voltage seen by the Buck Converter is:

$$V_{\text{BUCK(MAX)}} = V_{\text{AC-RMS(MAX)}} \times \sqrt{2}$$

### INDUCTOR SELECTION

The controlled off-time architecture of the LM3445 regulates the average current through the inductor (L2), and therefore the LED string current. The input voltage to the buck converter ($V_{\text{BUCK}}$) changes with line variations and over the course of each half-cycle of the input line voltage. The voltage across the LED string is relatively constant, and therefore the current through R4 is constant. This current sets the off-time of the converter and therefore the output volt-second product ($V_{\text{LED}} \times t_{\text{OFF}}$) remains constant. A constant volt-second product makes it possible to keep the ripple through the inductor constant as the voltage at $V_{\text{BUCK}}$ varies.

$$V_{\text{L(ON-TIME)}} = V_{\text{BUCK}} - (V_{\text{LED}} + V_{\text{DS(Q2)}} + I_{\text{L2}} \times R3)$$

Since the voltage across the MOSFET switch (Q2) is relatively small, as is the voltage across sense resistor R3, we can simplify this to approximately,

$$V_{\text{L(ON-TIME)}} = V_{\text{BUCK}} - V_{\text{LED}}$$

During the off-time, the voltage seen by the inductor is approximately:

$$V_{\text{L(OFF-TIME)}} = V_{\text{LED}}$$

The maximum voltage seen by the Buck Converter is:

$$V_{\text{BUCK}} = V_{\text{AC-RMS(MAX)}} \times \sqrt{2}$$

The value of $V_{\text{L(OFF-TIME)}}$ will be relatively constant, because the LED stack voltage will remain constant. If we rewrite the equation for an inductor inserting what we know about the circuit during the off-time, we get:

$$V_{\text{L(OFF-TIME)}} = V_{\text{LED}} = L \times \frac{\Delta i}{\Delta t}$$

Re-arranging this gives:

$$\Delta i \approx t_{\text{OFF}} \times \frac{V_{\text{LED}}}{L2}$$

From this we can see that the ripple current ($\Delta i$) is proportional to off-time ($t_{\text{OFF}}$) multiplied by a voltage which is dominated by $V_{\text{LED}}$ divided by a constant (L2).

These equations can be rearranged to calculate the desired value for inductor L2.

$$L2 \approx t_{\text{OFF}} \times \frac{V_{\text{LED}}}{\Delta i}$$

Where:

$$t_{\text{OFF}} = \left( 1 - \frac{1}{\eta} \times \frac{V_{\text{LED}}}{V_{\text{BUCK}}} \right) \times \frac{1}{f_{\text{SW}}}$$

Finally:

$$V_{\text{LED}} \left( 1 - \frac{1}{\eta} \times \frac{V_{\text{LED}}}{V_{\text{BUCK}}} \right) \times \frac{1}{f_{\text{SW}} \times \Delta i}$$

Refer to “Design Example” section of the datasheet to better understand the design process.
SETTING THE LED CURRENT

The LM3445 constant off-time control loop regulates the peak inductor current \( I_{L2} \). The average inductor current equals the average LED current \( I_{AVE} \). Therefore the average LED current is regulated by regulating the peak inductor current.

\[
I_{L2,PK} = I_{AVE} + \frac{\Delta I_L}{2}
\]

Or, the maximum, or “undimmed”, LED current would then be,

\[
I_{AVE(UNDIM)} = I_{L2,PK(UNDIM)} - \frac{\Delta I_L}{2}
\]

This is important to calculate because this peak current multiplied by the sense resistor \( R_3 \) will determine when the internal comparator is tripped. The internal comparator turns the control MOSFET off once the peak sensed voltage reaches 750 mV.

\[
I_{L2,PK(UNDIM)} = \frac{750 \text{ mV}}{R_3}
\]

**Current Limit:** Under normal circumstances, the trip voltage on the PWM comparator would be less than or equal to 750 mV, depending on the amount of dimming. However, if there is a short circuit or an excessive load on the output, higher than normal switch currents will cause a voltage above 1.27V on the ISNS pin which will trip the I-LIM comparator. The I-LIM comparator will reset the RS latch, turning off Q2. It will also inhibit the Start Pulse Generator and the COFF comparator by holding the COFF pin low. A delay circuit will prevent the start of another cycle for 180 \( \mu \text{s} \).

**VALLEY FILL CAPACITORS**

Determining voltage rating and capacitance value of the valley-fill capacitors:

The maximum voltage seen by the valley-fill capacitors is:

\[
V_{VF-CAP} = \frac{V_{ADMAX} \sqrt{2}}{\#\text{stages}}
\]

This is, of course, if the capacitors chosen have identical capacitance values and split the line voltage equally. Often a 20% difference in capacitance could be observed between like capacitors. Therefore a voltage rating margin of 25% to 50% should be considered.
Determining the capacitance value of the valley-fill capacitors:
The valley fill capacitors should be sized to supply energy to the buck converter ($V_{BUCK}$) when the input line is less than its peak divided by the number of stages used in the valley fill ($t_X$). The capacitance value should be calculated when the triac is not firing, i.e., when full LED current is being drawn by the LED string. The maximum power is delivered to the LED string at this time, and therefore the most capacitance will be needed.

From the above illustration and the equation for current in a capacitor, $i = C \times \frac{dV}{dt}$, the amount of capacitance needed at $V_{BUCK}$ will be calculated as follows:

At 60Hz, and a valley-fill circuit of two stages, the hold up time ($t_X$) required at $V_{BUCK}$ is calculated as follows. The total angle of an AC half cycle is 180° and the total time of a half AC line cycle is 8.33 ms. When the angle of the AC waveform is at 30° and 150°, the voltage of the AC line is exactly ½ of its peak. With a two stage valley-fill circuit, this is the point where the LED string switches from power being derived from AC line to power being derived from the hold up capacitors (C7 and C9). 60° out of 180° of the cycle or 1/3 of the cycle the power is derived from the hold up capacitors (1/3 x 8.33 ms = 2.78 ms). This is equal to the hold up time (dt) from the above equation, and dv is the amount of voltage the circuit is allowed to droop. From the next section ("Determining Maximum Number of Series Connected LEDs Allowed") we know the minimum $V_{BUCK}$ voltage will be about 45V for a 90V$_{AC}$ to 135V$_{AC}$ line. At 90V$_{AC}$ low line operating condition input, ½ of the peak voltage is 64V. Therefore with some margin the voltage at $V_{BUCK}$ can not droop more than about 15V (dv). (i) is equal to ($P_{OUT}$/V$_{BUCK}$), where $P_{OUT}$ is equal to ($V_{LED} \times I_{LED}$). Total capacitance (C7 in parallel with C9) can now be calculated. See "Design Example" section for further calculations of the valley-fill capacitors.

Determining Maximum Number of Series Connected LEDs Allowed:
The LM3445 is an off-line buck topology LED driver. A buck converter topology requires that the input voltage ($V_{BUCK}$) of the output circuit must be greater than the voltage of the LED stack ($V_{LED}$) for proper regulation. One must determine what the minimum voltage observed by the buck converter will be before the maximum number of LEDs allowed can be determined. Two variables will have to be determined in order to accomplish this.

1. AC line operating voltage. This is usually 90V$_{AC}$ to 135V$_{AC}$ for North America. Although the LM3445 can operate at much lower and higher input voltages a range is needed to illustrate the design process.

2. How many stages are implemented in the valley-fill circuit (1, 2 or 3).

In this example the most common valley-fill circuit will be used (two stages).

![FIGURE 19. Two Stage Valley-Fill $V_{BUCK}$ Voltage with no TRIAC Dimming](image)

The voltage at $V_{BUCK}$ with a valley fill stage of two will look similar to the waveforms of figure 22.

The purpose of the valley fill circuit is to allow the buck converter to pull power directly off of the AC line when the line voltage is greater than its peak voltage divided by two (two stage valley fill circuit). During this time, the capacitors within the valley fill circuit (C7 and C9) are charged up to the peak of the AC line voltage. Once the line drops below its peak divided by two, the two capacitors are placed in parallel and deliver power to the buck converter. One can now see that if the peak of the AC line voltage is lowered due to variations in the line voltage, or if the triac is firing at an angle above 90°, the DC offset ($V_{DC}$) will lower. $V_{DC}$ is the lowest value that voltage $V_{BUCK}$ will encounter.

$$V_{BUCK(MIN)} = \frac{V_{AC-RMS-PK} \sqrt{2} \times \sin(\theta)}{\text{#stages}}$$

Example:

Line voltage = 90V$_{AC}$ to 135V$_{AC}$

Valley-Fill = two stage

$$V_{BUCK(MIN)} = \frac{90 \sqrt{2} \times \sin(135°)}{2} = 45V$$

Depending on what type and value of capacitors are used, some derating should be used for voltage droop when the
capacitors are delivering power to the buck converter. When the triac is firing at 135° the current through the LED string will be small. Therefore the droop should be small at this point and a 5% voltage droop should be a sufficient derating. With this derating, the lowest voltage the buck converter will see is about 42.5V in this example.

To determine how many LEDs can be driven, take the minimum voltage the buck converter will see (42.5V) and divide it by the worst case forward voltage drop of a single LED.

Example: 42.5V/3.7V = 11.5 LEDs (11 LEDs with margin)

OUTPUT CAPACITOR
A capacitor placed in parallel with the LED or array of LEDs can be used to reduce the LED current ripple while keeping the same average current through both the inductor and the LED array. With a buck topology the output inductance (L2) can now be lowered, making the magnetics smaller and less expensive. With a well designed converter, you can assume that all of the ripple will be seen by the capacitor, and not the LEDs. One must ensure that the capacitor you choose can handle the RMS current of the inductor. Refer to manufacture’s datasheets to ensure compliance. Usually an X5R or X7R capacitor between 1 µF and 10 µF of the proper voltage rating will be sufficient.

SWITCHING MOSFET
The main switching MOSFET should be chosen with efficiency and robustness in mind. The maximum voltage across the switching MOSFET will equal:

\[ V_{DS(MAX)} = V_{AC-RMS(MAX)}\sqrt{2} \]

The average current rating should be greater than:

\[ I_{DS-MAX} = I_{LED(AVE)}(D_{MAX}) \]

RE-CIRCULATING DIODE
The LM3445 Buck converter requires a re-circulating diode D10 (see the Typical Application circuit figure 4) to carry the inductor current during the MOSFET Q2 off-time. The most efficient choice for D10 is a diode with a low forward drop and near-zero reverse recovery time that can withstand a reverse voltage of the maximum voltage seen at \( V_{BUCK} \). For a common 110VAC ± 20% line, the reverse voltage could be as high as 190V.

\[ V_D \geq V_{AC-RMS(MAX)}\sqrt{2} \]

The current rating must be at least:

\[ I_D = 1 \cdot (D_{MIN}) \times I_{LED(AVE)} \]

Or:

\[ I_D = \left(1 - \frac{V_{LED(MIN)}}{V_{BUCK(MAX)}}\right) \times I_{LED(AVE)} \]
Design Example
The following design example illustrates the process of calculating external component values.

Known:
1. Input voltage range (90V<sub>AC</sub> – 135V<sub>AC</sub>)
2. Number of LEDs in series = 7
3. Forward voltage drop of a single LED = 3.6V
4. LED stack voltage = (7 x 3.6V) = 25.2V

Choose:
1. Nominal switching frequency, f<sub>SW-TARGET</sub> = 250 kHz
2. I<sub>LED(AVE)</sub> = 400 mA
3. ΔI (usually 15% - 30% of I<sub>LED(AVE)</sub>) = (0.30 x 400 mA) = 120 mA
4. Valley fill stages (1,2, or 3) = 2
5. Assumed minimum efficiency = 80%

Calculate:
1. Calculate minimum voltage V<sub>BUCK</sub> equals:
   \[ V_{BUCK(MIN)} = \frac{90 \sqrt{2} \times \sin(135^\circ)}{2} = 45V \]
2. Calculate maximum voltage V<sub>BUCK</sub> equals:
   \[ V_{BUCK(MAX)} = 135 \sqrt{2} = 190V \]
3. Calculate t<sub>OFF</sub> at V<sub>BUCK</sub> nominal line voltage:
   \[ t_{OFF} = \frac{1 - \frac{1}{0.8} \times \frac{25.2V}{115 \sqrt{2}}}{(250 kHz)} = 3.23 \mu s \]
4. Calculate t<sub>ON(MIN)</sub> at high line to ensure that t<sub>ON(MIN)</sub> > 200 ns:
   \[ t_{ON(MIN)} = \frac{1 - \frac{1}{0.8} \times \frac{25.2V}{135 \sqrt{2}}}{1 - \frac{1}{0.8} \times \frac{25.2V}{135 \sqrt{2}}} \times 3.23 \mu s = 638 \text{ ns} \]
5. Calculate C11 and R4:
6. Choose current through R4: (between 50 µA and 100 µA)
   \[ R4 = \frac{V_{LED}}{I_{COLL}} = 360 \text{ kΩ} \]
7. Use a standard value of 365 kΩ
8. Calculate C11:
   \[ C11 = \frac{V_{LED}}{R4 \times 1.276} = 175 \text{ pF} \]
9. \[ L2 = \frac{25.2V \left(1 - \frac{1}{0.8} \times \frac{25.2V}{115 \sqrt{2}}\right)}{(350 kHz \times 0.1A)} = 580 \mu H \]
10. Use standard value of 120 µF
11. Calculate ripple current: 400 mA X 0.30 = 120 mA
12. Calculate inductor value at t<sub>OFF</sub> = 3 µs:
13. Choose C10: 1.0 µF 200V
14. Calculate valley-fill capacitor values: V<sub>AC</sub> low line = 90V<sub>AC</sub>, V<sub>BUCK</sub> minimum equals 60V (no triac dimming at maximum LED current). Set droop for 20V maximum at full load and low line.
   \[ i = C \frac{dv}{dt} \]
   \[ i \text{ equals } P_{OUT}/V_{BUCK} \text{ (270 mA), dV equals 20V, dt equals } 2.77 \text{ ms, and then } C_{TOTAL} \text{ equals 37 } \mu \text{F. Therefore } C7 = C9 = 22 \text{ } \mu \text{F} \]
LM3445 Design Example 1
Input = 90V\textsubscript{AC} to 135V\textsubscript{AC}, \(V_{\text{LED}} = 7 \times \text{HB LED String Application} @ 400\ mA\)
<table>
<thead>
<tr>
<th>Qty</th>
<th>Ref Des</th>
<th>Description</th>
<th>Mfr</th>
<th>Mfr PN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>U1</td>
<td>IC, CTRLR, DRVR-LED, MSOP10</td>
<td>NSC</td>
<td>LM3445MM</td>
</tr>
<tr>
<td>1</td>
<td>BR1</td>
<td>Bridge Rectifier, SMT, 400V, 800 mA</td>
<td>DiodesInc</td>
<td>HD04-T</td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>Common mode filter DIP4NS, 900 mA, 700 µH</td>
<td>Panasonic</td>
<td>ELF-11090E</td>
</tr>
<tr>
<td>1</td>
<td>L2</td>
<td>Inductor, SHLD, SMT, 1A, 470 µH</td>
<td>Coilcraft</td>
<td>MSS1260-474-KLB</td>
</tr>
<tr>
<td>1</td>
<td>L3, L4</td>
<td>Diff mode inductor, 500 mA 1 mH</td>
<td>Coilcraft</td>
<td>MSS1260-105KL-KLB</td>
</tr>
<tr>
<td>1</td>
<td>L5</td>
<td>Bead Inductor, 160Ω, 6A</td>
<td>Steward</td>
<td>H1206T161R-10</td>
</tr>
<tr>
<td>3</td>
<td>C1, C2, C15</td>
<td>Cap, Film, X2Y2, 12.5MM, 250V, 10% 10 nF</td>
<td>Panasonic</td>
<td>ECQ-U2A103ML</td>
</tr>
<tr>
<td>1</td>
<td>C3</td>
<td>Cap, X7R, 0603, 16V, 10%, 470 nF</td>
<td>MuRata</td>
<td>GRM188R71C474KA88D</td>
</tr>
<tr>
<td>1</td>
<td>C4</td>
<td>Cap, X7R, 0603, 16V, 10%, 100 nF</td>
<td>MuRata</td>
<td>GRM188R71C104KA01D</td>
</tr>
<tr>
<td>2</td>
<td>C5, C6</td>
<td>Cap, X5R, 1210, 25V, 10%, 22 µF</td>
<td>MuRata</td>
<td>GRM32ER61E226KE15L</td>
</tr>
<tr>
<td>2</td>
<td>C7, C9</td>
<td>Cap, AL, 200V, 105C, 20%, 33 µF</td>
<td>Epcos</td>
<td>B32521C3103J</td>
</tr>
<tr>
<td>1</td>
<td>C10</td>
<td>Cap, Film, 250V, 5%, 10 nF</td>
<td>Kemet</td>
<td>C1206F105K5RACTU</td>
</tr>
<tr>
<td>1</td>
<td>C12</td>
<td>Cap, X7R, 1206, 50V, 10%, 1.0 uF</td>
<td>Kemet</td>
<td>C0603C102K5RACTU</td>
</tr>
<tr>
<td>1</td>
<td>C11</td>
<td>Cap, COG, 0603, 100V, 5%, 120 pF</td>
<td>Kemet</td>
<td>C0603C223K5RACTU</td>
</tr>
<tr>
<td>1</td>
<td>C13</td>
<td>Cap, X7R, 0603, 50V, 10%, 1.0 nF</td>
<td>Kemet</td>
<td>C0603C223K5RACTU</td>
</tr>
<tr>
<td>1</td>
<td>C14</td>
<td>Cap, X7R, 0603, 50V, 10%, 22 nF</td>
<td>Kemet</td>
<td>C0603C223K5RACTU</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>Diode, ZNR, SOT23, 15V, 5%</td>
<td>OnSemi</td>
<td>BZX84C15LT1G</td>
</tr>
<tr>
<td>1</td>
<td>D2, D13</td>
<td>Diode, SCH, SOD123, 40V, 120 mA</td>
<td>NXP</td>
<td>BAS40H</td>
</tr>
<tr>
<td>4</td>
<td>D3, D4, D8, D9</td>
<td>Diode, FR, SOD123, 200V, 1A</td>
<td>Rohm</td>
<td>RF071M2S</td>
</tr>
<tr>
<td>1</td>
<td>D10</td>
<td>Diode, FR, SMB, 400V, 1A</td>
<td>OnSemi</td>
<td>MURS140T3G</td>
</tr>
<tr>
<td>1</td>
<td>D11</td>
<td>IC, SHNT, ADJ, SOT23, 2.5V, 0.5%</td>
<td>TI</td>
<td>TL431B1DBZR</td>
</tr>
<tr>
<td>1</td>
<td>D12</td>
<td>TVS, VBR = 209V</td>
<td>LittleFuse</td>
<td>P6SMB220CA</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>Resistor, 0603, 1%, 280 kΩ</td>
<td>Panasonic</td>
<td>ERJ-3EFK2803V</td>
</tr>
<tr>
<td>1</td>
<td>R2</td>
<td>Resistor, 1206, 1%, 100 kΩ</td>
<td>Panasonic</td>
<td>ERJ-8ENF1003V</td>
</tr>
<tr>
<td>1</td>
<td>R3</td>
<td>Resistor, 1210, 5%, 1.8Ω</td>
<td>Panasonic</td>
<td>ERJ-14RQJ1R8U</td>
</tr>
<tr>
<td>1</td>
<td>R4</td>
<td>Resistor, 0603, 1%, 576 kΩ</td>
<td>Panasonic</td>
<td>ERJ-3EKF5763V</td>
</tr>
<tr>
<td>1</td>
<td>R5</td>
<td>Resistor, 1206, 1%, 1.00 kΩ</td>
<td>Panasonic</td>
<td>ERJ-8ENF1001V</td>
</tr>
<tr>
<td>2</td>
<td>R6, R7</td>
<td>Resistor, 0805, 1%, 1.00 MΩ</td>
<td>Rohm</td>
<td>MCR10EZH1004</td>
</tr>
<tr>
<td>2</td>
<td>R8, R10</td>
<td>Resistor, 1206, 0.0Ω</td>
<td>Yageo</td>
<td>RC1206JR-070R</td>
</tr>
<tr>
<td>1</td>
<td>R9</td>
<td>Resistor, 1812, 0.0Ω</td>
<td>Yageo</td>
<td>RC0603JR-070RL</td>
</tr>
<tr>
<td>1</td>
<td>R11</td>
<td>Resistor, 0603, 0.0Ω</td>
<td>Yageo</td>
<td>RC0603JR-070RL</td>
</tr>
<tr>
<td>1</td>
<td>R12</td>
<td>Resistor, 0603, 1%, 33.2 kΩ</td>
<td>Panasonic</td>
<td>ERJ-3EKF3322V</td>
</tr>
<tr>
<td>1</td>
<td>R13</td>
<td>Resistor, 0603, 1%, 2.0 kΩ</td>
<td>Panasonic</td>
<td>ERJ-3EKF2001V</td>
</tr>
<tr>
<td>1</td>
<td>R14</td>
<td>Resistor, 0805, 1%, 3.3 MΩ</td>
<td>Rohm</td>
<td>MCR10EZH3304</td>
</tr>
<tr>
<td>1</td>
<td>RT1</td>
<td>Thermistor, 120V, 1.1A, 500 @ 25°C</td>
<td>Thermometrics</td>
<td>CL-140</td>
</tr>
<tr>
<td>2</td>
<td>Q1, Q2</td>
<td>XSTR, NFET, DPAK, 300V, 4A</td>
<td>Fairchild</td>
<td>FQD7N30TF</td>
</tr>
<tr>
<td>1</td>
<td>Q3</td>
<td>XSTR, PNP, SOT23, 300V, 500 mA</td>
<td>Fairchild</td>
<td>MMBTA92</td>
</tr>
<tr>
<td>1</td>
<td>Q5</td>
<td>XSTR, NFET, SOT23, 100V, 170 mA</td>
<td>Fairchild</td>
<td>BSS123</td>
</tr>
<tr>
<td>1</td>
<td>J1</td>
<td>Terminal Block 2 pos</td>
<td>Phoenix Contact</td>
<td>1715721</td>
</tr>
<tr>
<td>1</td>
<td>F1</td>
<td>Fuse, 125V, 1.25A</td>
<td>bel</td>
<td>SSQ 1.25</td>
</tr>
</tbody>
</table>
**TI/NATIONAL INTERIM IMPORTANT NOTICE**

Texas Instruments has purchased National Semiconductor. As of Monday, September 26th, and until further notice, products sold or advertised under the National Semiconductor name or logo, and information, support and interactions concerning such products, remain subject to the preexisting National Semiconductor standard terms and conditions of sale, terms of use of website, and Notices (and/or terms previously agreed in writing with National Semiconductor, where applicable) and are not subject to any differing terms and notices applicable to other TI components, sales or websites. To the extent information on official TI and National websites and business social networking media, etc., pertains to both TI and National-branded products, both companies’ instructions, warnings and limitations in the above-referenced terms of use apply.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Audio</td>
<td><a href="http://www.ti.com/audio">www.ti.com/audio</a></td>
<td>Communications and Telecom</td>
</tr>
<tr>
<td>Amplifiers</td>
<td>amplifier.ti.com</td>
<td>Computers and Peripherals</td>
</tr>
<tr>
<td>Data Converters</td>
<td>dataconverter.ti.com</td>
<td>Consumer Electronics</td>
</tr>
<tr>
<td>DSP</td>
<td>dsp.ti.com</td>
<td>Industrial</td>
</tr>
<tr>
<td>Clocks and Timers</td>
<td><a href="http://www.ti.com/clocks">www.ti.com/clocks</a></td>
<td>Medical</td>
</tr>
<tr>
<td>Logic</td>
<td>logic.ti.com</td>
<td>Space, Avionics and Defense</td>
</tr>
<tr>
<td>Power Mgmt</td>
<td>power.ti.com</td>
<td>Transportation and Automotive</td>
</tr>
<tr>
<td>Microcontrollers</td>
<td>microcontroller.ti.com</td>
<td>Video and Imaging</td>
</tr>
<tr>
<td>RF/IF and ZigBee® Solutions</td>
<td><a href="http://www.ti.com/lprf">www.ti.com/lprf</a></td>
<td><strong>TI E2E Community Home Page</strong></td>
</tr>
</tbody>
</table>

**Mailing Address:** Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

**Copyright© 2011 Texas Instruments Incorporated**